【CLAIMS】

1. A time-interleaved delta-sigma modulator for converting an analog signal to a digital signal, comprising

a plurality of channel blocks, of which the phase of a clock frequency is different, comprising a first adder, a second adder, and a comparator,

whereby an input signal is inputted to the first adder according to an each channel block's clock frequency, and an n'th channel block's output u_n of the first adder is inputted to the first adder and the second adder of an (n+2)'th channel block, and an n'th block's output v_n of the second adder is inputted to the second adder of an (n+2)'th block, and an output y_n that passes an n'th block's comparator is inputted to the first adder and the second adder of an (n+2)'th block. Therefore, a modulator of the present invention receives output of the each block's comparator sequentially and makes the final output y.

2. The modulator of claim 1, wherein the number of channel blocks is odd number greater than or equal to five(5).

3. The modulator of claim 1 or 2, when supposing the number of channel blocks is N, wherein a phase difference between n'th channel block and (n+1)'th channel block is 1/N of each the clock frequency.

4. A time-interleaved delta-sigma modulator for converting an analog signal to a digital signal, comprising

a plurality of channel blocks, of which the phase of a clock frequency is different, comprising a first adder, a second adder, and a comparator,

whereby an input signal is inputted to the first adder according to an each channel block's clock frequency, and an n'th channel block's output u_n of the first adder is inputted to the first adder and the second adder of an (n+4)'th channel block, and an n'th block's output v_n of the second adder is inputted to the second adder of an (n+4)'th block, and an output y_n that passes an n'th block's comparator is inputted to the first adder and the second adder of an (n+4)'th block. Therefore, a modulator of the present invention receives output of the each block's comparator sequentially and makes the final output y.

5. The modulator of claim 4, wherein the number of channel blocks is odd number greater than or equal to nine(9).

6. The modulator of claim 4 or 5, when supposing the number of channel blocks is N, wherein a phase difference between n'th channel block and (n+1)'th channel block is 1/N of each the clock frequency.